1 HP Insight Management WBEM CPU Provider Overview

Description

The HP Insight Management Web-Based Enterprise Management (WBEM) CPU provider implements and extends classes described in this document to model the system processors.

This provider implements the following profiles and installs the necessary files:

Profile Name	Organization	Version
HP CPU Profile (P00106)	HP WBEM TC	1.0.0
HP CPU Consolidated Status Profile (P00107)	HP WBEM TC	1.0.0
HP CPU Physical Asset Profile (P00108)	HP WBEM TC	1.0.0
HP Location Profile (P00124)	HP WBEM TC	1.0

Requirements

For each hardware architecture listed, this provider requires the following distributions

HP Integrity managed servers	SLES 10 and later
	RLEL 5.0 and later
HP ProLiant managed servers	SLES 11 and later
	RHEL 5.3 and later

Release History

Initial release with HP Insight Management Providers for Linux v2.0.

1-1 Setting Up the Provider

Installing the Provider

There are no special installation instructions for this provider. It is installed by default as part of the HP Insight Management WBEM providers.

Configuring the

This provider does not accept specific configuration adjustments beyond standard HP

Provider Insight Management WBEM support.

1-2 Using the Provider

Namespaces Supported by the Provider This provider returns instances in the `root/hpq` namespace.

Schema Supported by the Provider This provider returns instances in the root/hpq namespace.

This provider supports the following classes:

- `SMX_Processor`
- `SMX_ProcessorCapabilities`
- `SMX_ProcessorCore`
- `SMX_HardwareThread`
- `SMX_ProcessorCacheMemory`
- `SMX_SystemProcessor`
- `SMX_ProcessorElementCapabilities`
- `SMX_ProcessorCoreComponent`
- `SMX_HWThreadComponent`
- `SMX_AssociatedCacheMemory`
- `SMX_ProcessorCollection`
- `SMX_HostedProcessorCollection`
- `SMX_MemberOfProcessorCollection`
- `SMX_ProcessorChip`
- `SMX_RealizesProcessor`
- `SMX_SystemPhysicalProcessor`
- `SMX_ProcessorLocation`
- `SMX_ProcessorElementLocation`

The tables in the following sections describe the properties of the supported classes. The classes are categorized by the class or superclass that defines the property, the first column is the Property Name (including type and units) and the second column describes how the provider determines the properties implementation. When the Property Implementation value is a number, the number given is the default behavior and the Managed Object Format interpretation is within parenthesis. If other values are returned, a problem is indicated.

Unless otherwise noted, all of the property implementation values given are for HP ProLiant and HP Integrity (cellular and non-cellular) systems. The location related properties and implementation values are determined based on the server type so they may differ.

1-2-1 SMX_Processor Class

The `SMX_Processor` class extends the `CIM_Processor` class to model the system processors.

The following table lists the properties implemented.

Property Name	Property Implementation
`CIM_ManagedElement`	
`Caption`	`Processor in <physical locations>` For text representing the CPU location, refer to "Physical Location".

`Description`	*<processor brand string>* (<cpu> Family <*x*> Model *y* Stepping <*z*>)
	Where: *<processor brand string>* is the processor brand string, (<cpu> is the CPU architecture type, <*x*> is the processor family number, <*y*> is the processor model number and *z* is the processor stepping number.
	For example:
	`Intel(R) Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7)`
	`Manufacturer: Intel(R) Family: Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7)`

`ElementName`	`Processor in <physical locations>` For text representing the CPU location, refer to "Physical Location".
`CIM_ManagedSystemElement`	
`Name`	`Processor in <physical locations>` For text representing the CPU location, refer to "Physical Location".
`OperationalStatus`	`0` (Unknown) 2 (OK), when CPU is enabled and operational 5 (Predictive Failure), when IML error info logged for this CPU 6 (Error), when CPU is disabled via POST error `10` (Stopped), when CPU is disabled via RBSU

Property Name	Property Implementation
StatusDescriptions	StatusDescriptions[0] text per OperationalStatus[0]: Unknown OK Error Stopped Predictive Failure
HealthState	0 (Unknown), when OperationalStatus[0]=0 (Unknown) 5 (OK), when OperationalStatus[0]=2 (OK) 15 (Minor Failure), when OperationalStatus[0]=10 (Stopped) 20 (Major Failure), when OperationalStatus[0]=5 (Predictive Failure) 25 (Critical Failure), when OperationalStatus[0]=6 (Error)
CIM_LogicalElement	
CIM_EnabledLogicalElement	
EnabledState	2 (Enabled)
RequestedState	12 (Not Applicable)
EnabledDefault	2 (Enabled)
CIM_LogicalDevice	
SystemCreationClassName	SMX_ComputerSystem
SystemName	computer system name
CreationClassName	SMX_Processor
DeviceID	Proc <*n*> where *n* is the processor number.
CIM_Processor	

Property Name	Property Implementation
`CPUStatus`	1 (CPU Enabled) 2 (CPU Disabled by User using BIOS Setup) 3 (CPU Disabled By BIOS (POST Error)) 4 (CPU Idle) 7 (Other)
`Family`	Processor family number from SMBIOS For example, 179 for Intel(R) Xeon(TM)
`MaxClockSpeed`	maximum clock speed in MHz For example: `3600`
`CurrentClockSpeed`	current clock speed in MHz For example: `3066`
`DataWidth`	32 – for x86 processors 64 – for x64 processors
`AddressWidth`	32 – for x86 processors 64 – for x64 processors
`ExternalBusClockSpeed`	external bus clock speed in MHz For example: `533`

`Characteristics`	For x86 processors:
	`Characteristics[0]`
	3 (32-bit Capable)
	For x64 processors:
	`Characteristics[0]`
	3 (32-bit Capable)
	`Characteristics[1]`
	2 (64-bit Capable)

Property Name	Property Implementation
NumberOfEnabledCores	Number of enabled and operational cores for this processor For example: 1, 2, 4
Stepping	Stepping for processor
Role	Processor Role
UniqueID	Unique identifier for processor
HP_Processor	
SMX_Processor	

1-2-2 SMX_ProcessorCapabilities Class

The SMX_ProcessorCapabilities class extends the CIM_ProcessorCapabilities class to model the processor capabilities.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Processor Capabilities
Description	Processor Capabilities
CIM_Capabilities	
InstanceID	HPQ:SMX_ProcessorCapabilities:<*n*> Where: <*n*> is a unique number.
ElementName	Processor Capabilities
CIM_EnabledLogicalElementCapabilities	
ElementNameEditSupported	0 (False)
RequestedStatesSupported	none
CIM_ProcessorCapabilities	
NumberOfProcessorCores	number of processor cores For example: 1, 2, 4

Property Name	Property Implementation
NumberOfHardwareThreads	number of hardware threads For example: 1, 2
HP_ProcessorCapabilities	
SMX_ProcessorCapabilities	

1-2-3 SMX_ProcessorCore Class

The SMX_ProcessorCore class extends the CIM_ProcessorCore class to model the processor cores.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Processor:<p> Core:<*c*> Where: <*p*> is the processor number and <*c*> is the core number.
Description	<*processor brand string*> (<cpu> Family <*x*> Model <*y*> Stepping <*z*>) (Processor:<*p*> Core:<*c*>) Where: <*processor brand string*> is the processor brand string, <cpu> is the CPU architecture type, <*x*> is processor family number, <*y*> is processor model number, <*z*> is processor stepping number, <*p*> is the processor number, and <*c*> is the core number. For example: Manufacturer: Intel(R) Family: Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7) (Processor:1 – Core:2)
ElementName	Processor:<p> Core:<*c*> Where: <*p*> is the processor number and <*c*> is the core number.
CIM_ManagedSystemElement	
Name	Processor:<p> Core:<*c*> *W*here: <*p*> is the processor number and <*c*> is the core number.
OperationalStatus	0 (Unknown) 2 (OK), when CPU is enabled and operational 5 (Predictive Failure), when IML error info logged for this CPU 6 (Error), when CPU is disabled via POST error 10 (Stopped), when CPU is disabled via RBSU

Property Name	Property Implementation
StatusDescriptions	StatusDescriptions[0] text per OperationalStatus[0]: Unknown. OK Predictive Failure Error Stopped
HealthState	0 (Unknown), when OperationalStatus[0]=0 (Unknown) 5 (OK), when OperationalStatus[0]=2 (OK) 15 (Minor Failure), when OperationalStatus[0]=10 (Stopped) 20 (Major Failure), when OperationalStatus[0]=5 (Predictive Failure) 25 (Critical Failure), when OperationalStatus[0]=6 (Error)
CIM_LogicalElement	
CIM_EnabledLogicalElement	
EnabledState	2 (Enabled)
RequestedState	12 (Not Applicable)
EnabledDefault	2 (Enabled)
CIM_ProcessorCore	
InstanceID	HPQ:SMX_ProcessorCore Proc:<p> Core:<c> *W*here: <*p*> is the processor number and <*c*> is the core number.
CoreEnabledState	2 (Core Enabled)
Characteristics	For x86 processors: Characteristics[0]: 3 (32-bit Capable) For x64 processors: Characteristics[0]: 3 (32-bit Capable) Characteristics[1]: 2 (64-bit Capable)
HP_ProcessorCore	

Property Name	Property Implementation
Bootstrap	FALSE TRUE
SMX_ProcessorCore	

1-2-4 SMX_HardwareThread Class

The SMX_HardwareThread class extends the CIM_HardwareThread class to model the hardware threads.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Processor:<*p*> Core:<*c*> Thread:<*t*> Where: <*p*> is the processor number, <*c*> is the core number, and <*t*> is the thread number
Description	<*processor brand string*> (<cpu> Family <x> Model <y> Stepping <z> Processor:<*p*> Core:<*c*> Thread:<*t*>) Where: <*processor brand string*> is the processor brand string, (<cpu> is the cpu architecture type, <*x*> is the processor family number, <*y*> is the processor model number and <*z*> is the processor stepping number, <*p*> is the processor number, <*c*> is the core number, and <*t*> is the thread number. For example: Intel(R) Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7) Manufacturer: Intel(R) Family: Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7) (Processor:1 Core:2 Thread:3)
ElementName	Processor:<*p*> Core:<*c*> Thread:<*t*> Where: <*p*> is the processor number, <*c*> is the core number, and <*t*> is the thread number
CIM_ManagedSystemElement	
Name	Processor:<*p*> Core:<*c*> Thread:<*t*> Where: <*p*> is the processor number, <*c*> is the core number, and <*t*> is the thread number

Property Name	Property Implementation
OperationalStatus	0 (Unknown) 2 (OK), when CPU is enabled and operational 5 (Predictive Failure), when IML error info logged for this CPU 6 (Error), when CPU is disabled via POST error 10 (Stopped), when CPU is disabled via RBSU
StatusDescriptions	StatusDescriptions[0] text per OperationalStatus[0]: OK Error Stopped Predictive Failure
HealthState	0 (Unknown), when OperationalStatus[0]=0 (Unknown) 5 (OK), when OperationalStatus[0]=2 (OK) 15 (Minor Failure), when OperationalStatus[0]=10 (Stopped) 20 (Major Failure), when OperationalStatus[0]=5 (Predictive Failure) 25 (Critical Failure), when OperationalStatus[0]=6 (Error)
CIM_LogicalElement	
CIM_EnabledLogicalElement	
EnabledState	2 (Enabled)
RequestedState	12 (Not Applicable)
EnabledDefault	2 (Enabled)
CIM_HardwareThread	
InstanceID	HPQ:SMX_HardwareThread: Proc:<p> Core:<c> Thread:<t> Where: <*p*> is the processor number, <*c*> is the core number and <*t*> is the thread number
HP_HardwareThread	
SMX_HardwareThread	

1-2-5 SMX_CacheMemory Class

The SMX_CacheMemory class implements the HP_CacheMemory class, which extends CIM_Memory to model the processor caches.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Level <*x*> Data Cache where <*x*> is the cache level number Level <*x*> Instruction Cache where <*x*> is the cache level number Level <*x*> Unified Cache where <*x*> is the cache level number For example: Level 1 Data Cache Level 2 Unified Cache
Description	Level <*x*> Data Cache where <*x*> is the cache level number Level <*x*> Instruction Cache where <*x*> is the cache level number Level <*x*> Unified Cache where <*x*> is the cache level number For example: Level 1 Data Cache Level 2 Unified Cache
ElementName	Level <*x*> Data Cache where <*x*> is the cache level number Level <*x*> Instruction Cache where <*x*> is the cache level number Level <*x*> Unified Cache where <*x*> is the cache level number For example: Level 1 Data Cache Level 2 Unified Cache
CIM_ManagedSystemElement	
OperationalStatus	0 (Unknown) 2 (OK), when CPU is enabled and operational 5 (Predictive Failure), when IML error info logged for this CPU 6 (Error), when CPU is disabled via POST error 10 (Stopped), when CPU is disabled via RBSU
StatusDescriptions	StatusDescriptions[0] text per OperationalStatus[0]: Unknown OK Stopped Error Predictive Failure

Property Name	Property Implementation
HealthState	0 (Unknown), when OperationalStatus[0]=0 (Unknown) 5 (OK), when OperationalStatus[0]=2 (OK) 15 (Minor Failure), when OperationalStatus[0]=10 (Stopped) 20 (Major Failure), when OperationalStatus[0]=5 (Predictive Failure) 25 (Critical Failure), when OperationalStatus[0]=6 (Error)
CIM_LogicalElement	
CIM_EnabledLogicalElement	
EnabledState	5 (Not Applicable)
RequestedState	12 (Not Applicable)
EnabledDefault	2 (Enabled)
CIM_LogicalDevice	
SystemCreationClassName	SMX_ComputerSystem
SystemName	Computer system name
CreationClassName	SMX_CacheMemory
DeviceID	Proc <*p*>, Level <*x*> <*type*> Cache Where: <*p*> is the processor number, <*x*> is the cache level number, and <*type*> is the cache type (Data, Instruction, or Unified) Proc <*p*>, Core <*c*>, Level <*x*> <*type*> Cache Where: <*p*> is the processor number, <*x*> is the cache level number, and <*type*> is the cache type (Data, Instruction, or Unified) For example: Proc 1, Level 1 Data Cache For example: Proc 1, Core 2, Level 2 Unified Cache
CIM_StorageExtent	
BlockSize	1 – number of bytes in a block
NumberOfBlocks	Number of blocks in this cache For example: 8192
Primordial	0 (False)

Property Name	Property Implementation
CIM_Memory	
HP_CacheMemory	
SMX_ProcessorCacheMemory	

1-2-6 SMX_SystemProcessor Class

The SMX_SystemProcessor class extends the CIM_SystemDevice class and associates the SMX_ComputerSystem instance and SMX_Processor instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Component	
CIM_SystemComponent	
CIM_SystemDevice	
HP_SystemProcessor	
SMX_SystemProcessor	
GroupComponent	References SMX_ComputerSystem
PartComponent	References SMX_Processor

1-2-7 SMX_ProcessorElementCapabilities Class

The SMX_ProcessorElementCapabilities class extends the CIM_ElementCapabilities class and associates SMX_Processor and SMX_ProcessorCapabilities instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ElementCapabilities	
HP_ProcessorElementCapabilities	
SMX_ProcessorElementCapabilities	
ManagedElement	References SMX_Processor
Capabilities	References SMX_ProcessorCapabilities

1-2-8 SMX_ProcessorCoreComponent Class

The SMX_ProcessorCoreComponent class extends the CIM_ConcreteComponent class and associates an SMX_Processor instance withSMXP_ProcessorCore instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Component	
CIM_ConcreteComponent	
HP_ProcessorCoreComponent	
SMX_ProcessorCoreComponent	
GroupComponent	References SMX_Processor
PartComponent	References SMX_ProcessorCore

1-2-9 SMX_HWThreadComponent Class

The SMX_HWThreadComponent class extends the CIM_ConcreteComponent class and associates an SMX_ProcessorCore instance with SMX_HardwareThread instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Component	
CIM_ConcreteComponent	
HP_HWThreadComponent	
SMX_HWThreadComponent	
GroupComponent	References SMX_ProcessorCore
PartComponent	References SMX_HardwareThread

1-2-10 SMX_AssociatedProcessorCacheMemory Class

The SMX_AssociatedProcessorCacheMemory class extends the CIM_AssociatedCacheMemory class. The SMX_AssociatedProcessorCacheMemory class associates an SMX_Processor instance with an SMX_CacheMemory instance.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Dependency	
CIM_AssociatedMemory	
CIM_AssociatedCacheMemory	
Level	0 (Unknown) 1 (Other) 2 (Not Applicable) 3 (Primary) 4 (Secondary) 5 (Tertiary)
WritePolicy	0 (Unknown) 1 (Other) 2 (Write Back) 3 (Write Through) 4 (Varies with Address) 5 (Determination Per I/O)
CacheType	0 (Unknown) 1 (Other) 2 (Instruction) 3 (Data) 4 (Unified)
LineSize	Cache line size in bytes
ReadPolicy	0 (Unknown) 1 (Other) 2 (Read) 3 (Read-Ahead) 4 (Read and Read-Ahead) 5 (Determination Per I/O)

Property Name	Property Implementation
Associativity	0 (Unknown) 1 (Other) 2 (Direct Mapped) 3 (2-way Set-Associative) 4 (4-way Set-Associative) 5 (Fully Associative) 6 (8-way Set-Associative) 7 (16-way Set-Associative)
HP_AssociatedCacheMemory	
SMX_AssociatedProcessorCacheMemory	
Antecedent	References SMX_CacheMemory
Dependent	References SMX_Processor

1-2-11 SMX_ProcessorCollection Class

The SMX_ProcessorCollection class extends the HP_GroupSystemSpecificCollection class.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Description	A collection of processor packages with group aggregate status
ElementName	SMX_ProcessorCollection
CIM_Collection	
CIM_SystemSpecificCollection	
InstanceID	HPQ:SMX_ProcessorCollection-1
HP_GroupSystemSpecificCollection	
Caption	Processor Package Collection

Property Name	Property Implementation
GroupOperationalStatus	GroupOperationalStatus[0] contains the processors consolidated status. GroupOperationalStatus[0] will contain one of the following: 0 (Unknown) 1 (Other) 2 (OK) 3 (Degraded) 5 (Predictive Failure) 6 (Error) 10 (Stopped) The status values of the processors that make up the overall group operational status are contained in GroupOperationalStatus[1-n]. See the descriptions for OperationalStatus for members of the processor collection for the list of possible values.
GroupStatusDescriptions	GroupStatusDescriptions[0] text per GroupOperationalStatus[0]: Unknown Other OK Degraded Predicted Failure Failed Stopped The status descriptions of the processors that make up the overall operational status are contained in OperationalStatus[1-n]. See the descriptions for GroupStatusDescriptions for members of the processor collection for the list of possible values.
HP_ProcessorCollection	
SMX_ProcessorCollection	

1-2-12 SMX_HostedProcessorCollection Class

The SMX_HostedProcessorCollection class extends the HP_GroupHostedCollection class and associates the SMX_ComputerSystem instance with the SMX_ProcessorCollection instance.

The following table lists the properties implemented.

Property Name	Property Implementation

Property Name	Property Implementation
CIM_Dependency	
CIM_HostedDependency	
CIM_HostedCollection	
HP_GroupHostedCollection	
SMX_HostedProcessorCollection	
Antecedent	References SMX_ComputerSystem
Dependent	References SMX_ProcessorCollection

1-2-13 SMX_MemberOfProcessorCollection Class

The SMX_MemberOfProcessorCollection class extends the CIM_MemberOfCollection class and associates the SMX_ProcessorCollection instance with an SMX_Processor instance.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_MemberOfCollection	
SMX_MemberOfProcessorCollection	
Member	References SMX_Processor
Collection	References SMX_ProcessorCollection

1-2-14 SMX_ProcessorChip Class

The SMX_ProcessorChip class extends the CIM_Chip class to model the physical processor chip.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Processor in *<physical locations>* For text representing the CPU location, refer to "Physical Location".
CIM_ManagedSystemElement	
Name	Processor in *<physical locations>*

Property Name	Property Implementation
	For text representing the CPU location, refer to "Physical Location".
OperationalStatus	0 (Unknown) 2 (OK), when CPU is enabled and operational 5 (Predictive Failure), when IML error info logged for this CPU 6 (Error), when CPU is disabled via POST error 10 (Stopped), when CPU is disabled via RBSU
StatusDescriptions	StatusDescriptions[0] text per OperationalStatus[0]: Unknown. OK Predicted Failiure Error Stopped
HealthState	0 (Unknown), when OperationalStatus[0]=0 (Unknown) 5 (OK), when OperationalStatus[0]=2 (OK) 15 (Minor Failure), when OperationalStatus[0]=10 (Stopped) 20 (Major Failure), when OperationalStatus[0]=5 (Predictive Failure) 25 (Critical Failure), when OperationalStatus[0]=6 (Error)
CIM_PhysicalElement	
Tag	*<manufacturer string> <family string> <physical_location>* Where: *<manufacturer string>* is the processor manufacturing name, *<family string>* is the processor family name string and *<physical location >*is the CPU location. For text representing the CPU location, refer to "Physical Location".

Property Name	Property Implementation
Description	<*processor brand string*> (<*cpu*> Family <*x*> Model <*y*> Stepping <*z*>) Where : <*processor brand string*> is the processor brand string, <*cpu*> is the CPU architecture type, <*x*> is the processor family number, <*y*> is the processor model number and <*z*> is the processor stepping number. For example: Manufacturer: Intel(R) Family: Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7) x86 Family 15 Model 2 Stepping 7
CreationClassName	SMX_ProcessorChip
ElementName	Processor in <*physical locations*> For text representing the CPU location, refer to "Physical Location".
Manufacturer	Processor manufacturer string from SMBIOS For example: Intel
Model	Model <*y*> Where: <*y*> is the processor model number
Version	Model <*y*> Stepping <*z*> Where: <*y*> is the processor model number and <*z*> is the processor stepping number
PoweredOn	0 (False) – if CPU is disabled via RBSU or POST error 1 (True) – if CPU is enabled
CanBeFRUed	0 (False) 1 (True)
CIM_PhysicalComponent	
RemovalConditions	3 (Removable When Off)
CIM_Chip	
HP_ProcessorChip	
ProcessorChipRevision	Stepping <*z*>

Property Name	Property Implementation
	Where: <z> is the processor stepping number
SMX_ProcessorChip	

1-2-15 SMX_RealizesProcessor Class

The SMX_RealizesProcessor class extends the CIM_Realizes class and associates SMX_Processor instances with SMX_ProcessorChip instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Dependency	
CIM_Realizes	
HP_RealizesProcessor	
SMX_RealizesProcessor	
Antecedent	References SMX_ProcessorChip
Dependent	References SMX_Processor

1-2-16 SMX_SystemPhysicalProcessor Class

The SMX_SystemPhysicalProcessor class extends the CIM_Container class and associates the SMX_ComputerSystemChassis instance with SMX_ProcessorChip instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_Component	
CIM_Container	
HP_SystemPhysicalProcessor	
SMX_SystemPhysicalProcessor	
GroupComponent	References SMX_ComputerSystemChassis
PartComponent	References SMX_ProcessorChip

1-2-17 SMX_ProcessorLocation Class

The SMX_ProcessorLocation class implements the HP_Location class which extends the class CIM_Location.

For ProLiant systems, processor location is denoted by the use of a slot number designator and a socket number designator. Either value might be zero, depending on the system:

- On older ProLiant systems, the processors are mounted on processor boards that fit in slots in the system. The slot number designator indicates the processor board slot where the processor is located. A socket number designator value of zero indicates one processor is mounted on a processor board. A nonzero socket number designator indicates the multiple processor board sockets where a processor is located.
- On modern ProLiant systems, processors are mounted in sockets on the system board. When the slot number designator is zero, the processors are located on the system board

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ManagedElement	
Caption	Processor in *<physical locations>* For text representing the CPU location, refer to "Physical Location".
Description	*<processor brand string>* (*<cpu>* Family *<x>* Model *<y>* Stepping *<z>*) Where : *<processor brand string>* is the processor brand string, *<cpu>* is the CPU architecture type, *<x>* is the processor family number, *<y>* is the processor model number and *<z>* is the processor stepping number. For example: Intel(R) Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7) Manufacturer: Intel(R) Family: Xeon(TM) CPU 3.06GHz (x86 Family 15 Model 2 Stepping 7)
ElementName	Processor in *<physical locations>* For text representing the CPU location, refer to "Physical Location".
CIM_Location	
Name	HPQ:SMX_ProcessorLocation:<a> Where: *<a>* is the slot number HPQ:SMX_ProcessorLocation:<b> Where: <b> is the socket number HPQ:SMX_ProcessorLocation:<a:b> Where: *<a>* is the slot number and *<b>* is the socket number

Property Name	Property Implementation
PhysicalPosition	<*a*> Where: <*a*> is the slot number (when no socket number exists) <*b*> Where: <*b*> is the socket number (when no slot number exists) <*a*:*b*> Where: <*a*> is the slot number and <*b*> is the socket number For text representing the CPU location, refer to "Physical Location".
HP_Location	
ElementLocationTag	<*physical locations*> For text representing the CPU location, refer to "Physical Location".
ElementLocationTagDesc	14 (Processor Module)
LocationInformation	If only socket number is available: LocationInformation[0]: <*b*> Where: <*b*> is the socket number If only slot number is available: LocationInformation[0]:<*a*> Where: <*a*> is the slot number If both socket and slot numbers are available: LocationInformation[0]: <*b*> Where: <*b*> is the socket number LocationInformation[1]: <*a*> Where: <*a*> is the slot number.
LocationInfoDesc	If only socket number is available: LocationInfoDesc[0]: 4 (Socket) indicates that the first element of the LocationInformation array contains the socket number If only slot number is available: LocationInfoDesc[0]: 0 (Slot), indicates that the second element of the LocationInformation array contains the slot number If both socket and slot numbers are available: LocationInfoDesc[0]: 4(Socket), indicates that the first element of the LocationInformation array contains the socket number LocationInfoDesc[1]: 0 (Slot), indicates that the second element of the LocationInformation array contains the slot number
HP_ProcessorLocation	

Property Name	Property Implementation
SMX_ProcessorLocation	

1-2-18 SMX_ProcessorElementLocation Class

The SMX_ProcessorElementLocation class extends the HP_ElementLocation class and associates SMX_ProcessorChip instances with SMX_ProcessorLocation instances.

The following table lists the properties implemented.

Property Name	Property Implementation
CIM_ElementLocation	
HP_ElementLocation	
SMX_ProcessorElementLocation	
Element	References SMX_ProcessorChip
PhysicalLocation	References SMX_ProcessorLocation

1-3 Physical Location

The Processor Physical Location is a string representing the physical location of a physical CPU module or chip. This string should represent the physical location of the device with which an end-user can uniquely locate the device. Most of these strings will be represented in customer documentation, silkscreen labels, or hood tags.

The following table lists the properties implemented. Any combination of the following applicable descriptors could be used to better define the device location.

All Systems	HP Integrity Cellular Servers	HP Blade Servers in C3000/C7000 Enclosures
CPUSocket=<*socket_num*> on System Mainboard	Cabinet=<*cell_or_blade_cabinet_num*>	–
ProcessorBoard=<*board_num*>	Cell=<*cell_num*>	Blade=<*blade_num*>
System Mainboard(referring to motherboard)	–	–
CPUSocket=<*socket_num*> on ProcessorBoard=<board_*num*>	–	–

1-4 Provider Indications

Indications Generated by the Provider

The SMX CPU Provider generates WBEM indications described in the following sections.

1-4-1 Common Properties for Provider Indications

The following table describes the properties that are common to all of the SMX CPU Provider indications that are implemented for HP server platforms where available:

Property Name	Property Implementation
CIM_Indication	
IndicationIdentifier	GUID string generated at the time of indication.
IndicationTime	Time of indication.
CIM_AlertIndication	
EventTime	Time of the event or time of the indication if event time unknown.
SystemName	SMX_ComputerSystem.Name
SystemCreationClassName	SMX_ComputerSystem.CreationClassName
HP_AlertIndication	
ProviderVersion	Provider Version in the format *VV.UU.FF*. For example: 01.05.00
NetworkAddresses	Contains a list of all the IP addresses of the computer system generating the indication.
OSType	On ESX, 39 (VM). On Linux, 36 (Linux).
OSVersion	The operating system version of the computer system generating the indication in the following format: *<major>.<minor>.<build>*
SystemFirmwareVersion	Array of firmware versions of the computer system generating the indication.
SystemSerialNumber	Serial number of the computer system generating the indication.
SystemProductID	Product ID of the computer system generating the indication.
SystemModel	Model name of the computer system generating the indication.

Property Name	Property Implementation
SystemGUID	Platform GUID of the computer system generating the indication.

1-4-2 HP_DeviceIndication: Processor Failed POST

Property Name	Property Implementation
CIM_Indication	
PerceivedSeverity	4 (Minor)
CIM_AlertIndication	
Description	CPU Failed Power on Self Test (POST)
AlertType	5 (Device Alert)
EventID	1
EventCategory	2 (Processor)
ProviderName	HP Processor
RecommendedActions	Replace the failed processor
HP_AlertIndication	
Summary	CPU Failed Power on Self Test (POST)
ProbableCause	1 (Other)

1-4-3 HP_DeviceIndication: Processor Disabled by BIOS or EFI

Property Name	Property Implementation
CIM_Indication	
PerceivedSeverity	4 (Minor)
CIM_AlertIndication	
Description	CPU has been disabled by BIOS or EFI
AlertType	5 (Device Alert)
EventID	2
EventCategory	2 (Processor)

Property Name	Property Implementation
ProviderName	HP Processor
RecommendedActions	Enable processor via BIOS or EFI
HP_AlertIndication	
Summary	CPU has been disabled by BIOS or EFI
ProbableCause	1 (Other)

1-4-4 HP_DeviceIndication: Processor Predicted to fail

Property Name	Property Implementation
CIM_Indication	
PerceivedSeverity	4 (Minor)
CIM_AlertIndication	
Description	CPU Predictive Failure Notification
AlertType	5 (Device Alert)
EventID	3
EventCategory	2 (Processor)
ProviderName	HP Processor
RecommendedActions	Replace the failing processor.
HP_AlertIndication	
Summary	CPU Predictive Failure detected
ProbableCause	1 (Other)